REMARKS

The Examiner is thanked for the examination of the application. In view of the foregoing amendments and the remarks that follow, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections. A Request for Continued Examination is submitted herewith.

Claims 1, 4, 5, 8, and 9 have been rejected under 35 USC 103(a) as being unpatentable over USP 6,952,492, hereinafter *Tanaka*, in view of EP 0643293 A1, hereinafter *Toshiba*.

In order to more clearly distinguish the claims over the applied prior art, claims 1, 5, 8, and 9 have been amended to recite that each of the four corner pattern portions (represented in the preferred embodiments as 17a-17d) has two perpendicular edges defining the respective corner portion and an L-shaped outer area (represented in the preferred embodiments as $17Y_1$-$17Y_4$) surrounding the perpendicular edges. And, each of the four side pattern portions (represented in the preferred embodiments as 17e-17h) has a straight edge portion defining a vertical edge or a horizontal edge and an outer edge portion ($17X_1$-$17X_4$) of the straight edge portion. However, the present invention is not limited to the preferred disclosed embodiments.

As a result, the present invention is clearly distinguished over the cited prior art.

By constituting each of the four corner portions (17a-17d) and each of the four side pattern portions (17f-17i) of the master pattern (17) as described above, the nine standard pattern portions (17a-17i) of the master pattern (17) can be easily

matched with the inspection view areas, respectively, without requiring severe positional alignment.

See, for example, paragraph [0039] of the published application, which, in describing the prior art states:

> That is, assume that the standard pattern portion not containing information on the edge shape or its exterior out area of the semiconductor chip 16 is to be positionally aligned with the corner portion 16a of the semiconductor chip 16, for example. Since this standard pattern portion contains no exterior area information, the image data of the inspection area information largely differs from that of the standard pattern portion if the standard pattern portion is even slightly deviated outwardly from the semiconductor chip 16. Because, the image information in the exterior area caused by this deviation is taken in...

However, this problem is overcome by the present invention, as described in the second half of paragraph [0039]:

> To the contrary, according to the present invention of this application, since the information on the edge shapes and the exterior areas are correspondingly contained in the standard pattern portions 17a to 17h on the peripheral portion excluding the central pattern portion 17i, no severe positional alignment needs not be done unlike in the prior art. Therefore, the peripheral standard pattern portions 17a to 17h can be positionally aligned at a relatively large allowable error, that is, with the same allowable error as in the case of the central pattern portion 17i, so that erroneous judgment due to the error in this alignment is avoided. As a result, the occurrence of the erroneous judgment due to the error in arrangement of the standard pattern portion 17a to 17h constituting the master pattern 17 is avoided, and the effective surface inspection can be performed.

On the other hand, in *Tanaka*, five checking positions including four corners and a center are disclosed. However, the technology disclosed in *Tanaka* relates to a method and apparatus for inspecting a semiconductor device in which failure occurrence conditions on a whole wafer are estimated by calculating the statistics of potential contrasts in pattern sections from sampled images throughout. Defective conditions of a process are detected at an early stage with the help of time series data of the estimate result.

Therefore, *Tanaka* does not disclose that each of the four corner pattern portions has two perpendicular edges defining the respective corner portion and an L-shaped outer area surrounding the perpendicular edges and each of the four side pattern portions has a straight edge portion defining a vertical edge or a horizontal edge and an outer edge portion of the straight edge portion as in the present invention.

Moreover, the technology described in *Toshiba* relates to a pattern defect inspection method and an apparatus for detecting a defect of an object to be inspected. *Toshiba* operates by comparing reference image data and inspection image data obtained by optically scanning the object to be inspected. However, *Toshiba* also does not disclose that each of the four corner pattern portions has two perpendicular edges and each of the four side pattern portions has a straight edge portion defining a vertical edge or a horizontal edge and an outer edge portion of the straight edge portion as the present invention.

Therefore, Applicants submit that the present invention significantly differs from the technology described in *Tanaka* and *Toshiba* in the structure and technical effect, and is not easily made based on the technical matters set forth in the applied art. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejections.

In the event that there are any questions concerning this Amendment, or the application in general, the Examiner is respectfully urged to telephone the undersigned attorney so that prosecution of the application may be expedited.

Respectfully submitted,

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